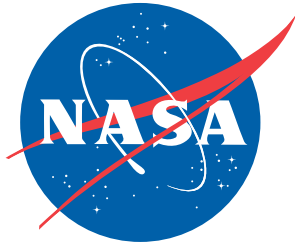# Power MOSFET Thermal Instability Operation Characterization Support

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April 2010

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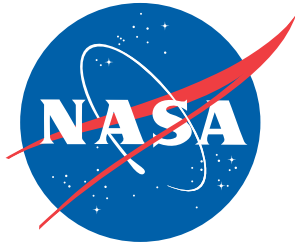
Power MOSFET Thermal Instability Operation Characterization Support

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Nomenclature
FET   Field-Effect Transistor
GSFC   Goddard Space Flight Center
IEEE   Institute of Electrical & Electronics Engineers, Incorporated
IR   International Rectifier
JPL   Jet Propulsion Lab
JWST   James Webb Space Telescope
MMS   Magnetospheric Multiscale
MOSFET   Metal-Oxide Semiconductor Field-Effect Transistor
PC   Printed Circuit
SOA   Safe Operating Area

1.0   Introduction

Metal-oxide semiconductor field-effect transistors (MOSFETs) are used extensively in flight hardware and ground support equipment. In the quest for faster switching times and lower "on resistance," the MOSFETs designed from 1998 to the present have achieved most of their intended goals. Unfortunately, along with the good (higher power efficiencies and lower total mass in DC – DC converters, and high speed switches) has come the bad. In the quest for lower on resistance and higher switching speeds, the designs now being produced allow the charge-carrier dominated region (once small and outside of the area of concern) to become important and inside the safe operating area (SOA). The charge-carrier dominated region allows more current to flow as the temperature increases. The higher temperatures produce more current resulting in the beginning of thermal runaway. While the problem may start with the entire part, as the runaway progresses, a hot spot starts to form then becomes smaller in size. With more power in a smaller area the temperature rises even higher and faster. The smaller hot spot produces higher temperatures resulting in the failure of the part. Temperatures above 450ºC on any location within the part will cause the metals to begin migrating causing a fatal short.

Earlier MOSFETs were primarily run in the mobility-charge dominated region. While maintaining the same gate voltage, the mobility-charge dominated region cuts back on the current as the temperatures increase, in turn decreasing the current allowing for the system to have negative feedback away from the thermal runaway. Indeed when the new power MOSFETs have high gate voltages the parts are mobility-charge dominated. It has been the unspoken intent of the manufacturers to keep the MOSFETs in the mobility-charge dominated region, as they are when used as a high speed switch. The older parts have a charge-carrier dominated area. The area, however, is outside the normal SOA and failures occur for other reasons.

2.0   Background

During a recent board-level test of a radiation protection circuit in a power supply being built for the James Webb Space Telescope (JWST), a MOSFET quickly failed. The protection circuit should have sheltered the MOSFET instead of causing it to fail. Since the test was unusual, it was originally believed that the test itself induced the failure. A replacement MOSFET was installed and the test was rerun. The second MOSFET failed during diagnostic electrical probing. Review of the parts revealed that both had failed from thermal stress caused by an apparent thermal runaway. Temperature internal to the parts had to have exceeded 450ºC as indicated by melted internal aluminum spheres (Figure 1) and discoloration of the parts' die in localized areas (Figure 2).
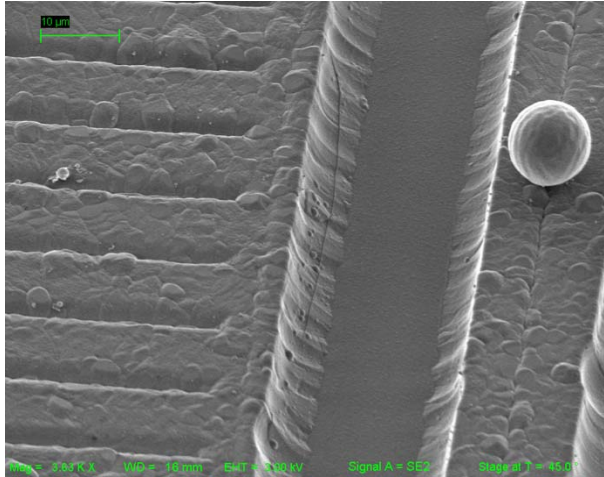
Figure 1. Aluminum sphere formed from overheating.
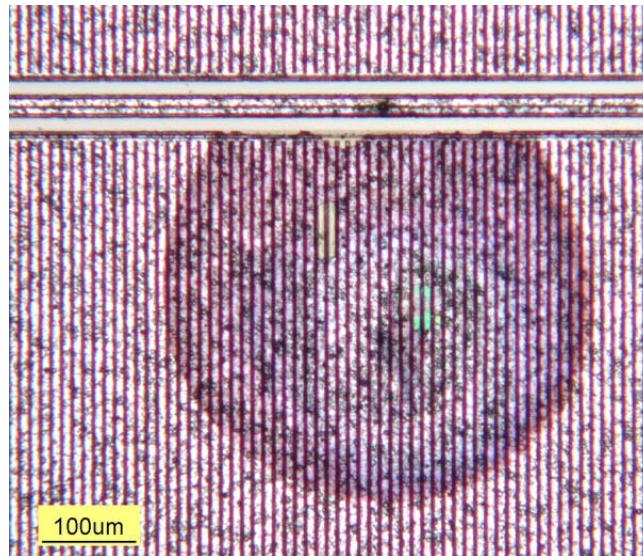
Figure 2. Failure area of first MOSFET.

The "bulls-eye" pattern in the photographs led to suggestion that the failure mode for the two MOSFETs were common and was caused by the MOSFETs being placed in a thermal runaway condition when the gate voltage was low yet well within the SOA for the MOSFETs. This problem, known as "thermal instability," has been known to the automotive industry since the year 1997 (when advanced very fast switching MOSFET devices became available). Numerous published articles in MOSFET engineering literature acknowledge the problem, but is not recorded in application notes or in the parts' data sheets from the manufacturers. When questioned, the manufacturer, International Rectifier (IR), responded that they believed their parts were only being used in a switching mode operation (high gate voltage) and not in areas where the gate voltage was low.

2.1   MOSFET Failures Inside the Advertised SOA

A consultant was requested to review the problem felt to be involving the thermal runaway. This same problem was observed at the Jet Propulsion Laboratory (JPL) in 2003 and was labeled as a "Thermal Instability inside the advertised SOA." The 2003 JPL failure had built a "Protection Circuit" and destroyed the MOSFET every time the circuit was tested. JPL looked into this destruction, talked to the

manufacturer, and discovered the auto industry had found the problem in 1997. JPL then reverted to "older parts," and trusted the manufacturer to advertise the problem; however, this never occurred.

The automobile industry found MOSFETs would short when used in protection circuits and variable speed fan controllers. Manufacturers, the automobile industry, and the Institute of Electrical & Electronics Engineers, Inc. (IEEE) produced papers on the problem from 2000 to present.

Goddard Space Flight Center (GSFC) identified the problem in October 2008 during two different projects. Magnetospheric Multiscale (MMS) learned of the thermal runaway inside the advertised SOA during an MMS Spacecraft Power Review. JWST learned of this problem during bench testing of a power supply "protection circuit."

Thermal runaway is a problem affecting a wide range of modern MOSFETs from more than one manufacturer. Older parts also show thermal runaway, but well outside the SOA. Thermal runaway is currently over a larger area of the $V_d - I_d$ plane and inside the advertised SOA affecting most modern power MOSFETs. Refer to Figures 3 and 4.
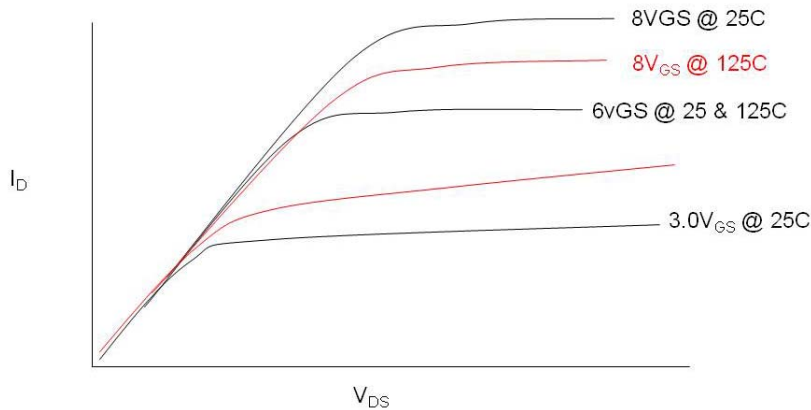

Figure 3. $V_{GS} - V_{DS}$ Planes.
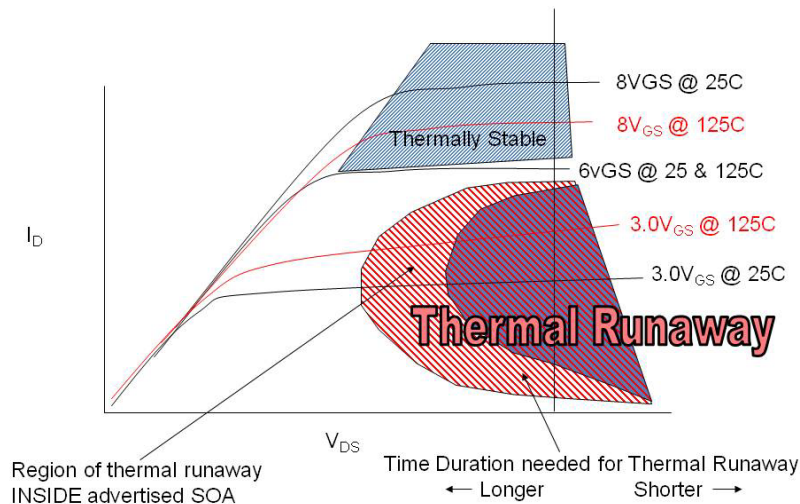
Figure 4. Maximum safe voltage.

From Figures 3 and 4 it can be seen that as the V_{DS}, or the thermal resistance, goes up and the SOA goes down.

3

If the V_{DS} and thermal resistance of the system is low enough no problem occurs. However, for any given V_{DS} as the system moves away from the ideal, the thermal resistance increases and the thermal instability begins to be a problem.

All of the above has been made with the assumption that time is not involved and that the system is static. This is the starting point for the first analysis; however, the thermal resistance is time dependant. The failure mechanism reverts to a single cell reaching a temperature that causes the part to fail. If the pulse of power is short enough, the temperature does not have time to reach a dangerous level. This is effectively why the part can withstand being turned on and off repeatedly; its intended function. If, however, the pulse of power is longer, the part has time to reach failure temperatures, even with lower power levels.

With knowing the thermal resistance and where the voltages become critical, it is possible to begin review of the SOA for the parts in question. The standard SOA chart (see Figure 5) is composed of four sets of boundaries. They are:

1. The boundary defined by the internal resistance of the part which is physically impossible to exceed.

2. The maximum allowable current the part can tolerate (bond wire fusing being a limiting factor).

3. The maximum reverse voltage, mainly limited by the voltage breakdown of the diffusion layer.

4. Maximum allowable power in the part caused by normal switching mode operation and heat dissipation.

Figure 5. Standard SOA chart.

In Figure 5, the area showing a thermal instability has not been included. To show the region of instability requires a fifth boundary, as shown in Figure 6, and changes the shape of the maximum power limit.
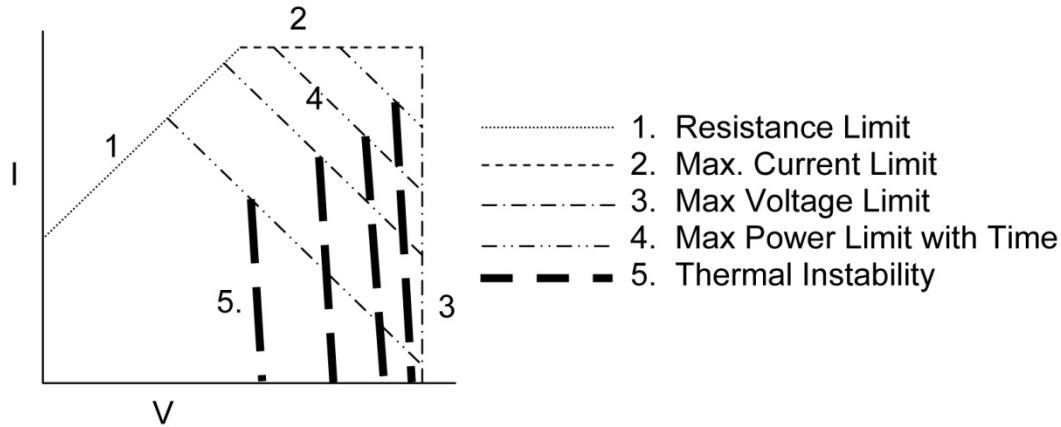
Figure 6. Standard SOA chart including region of instability.

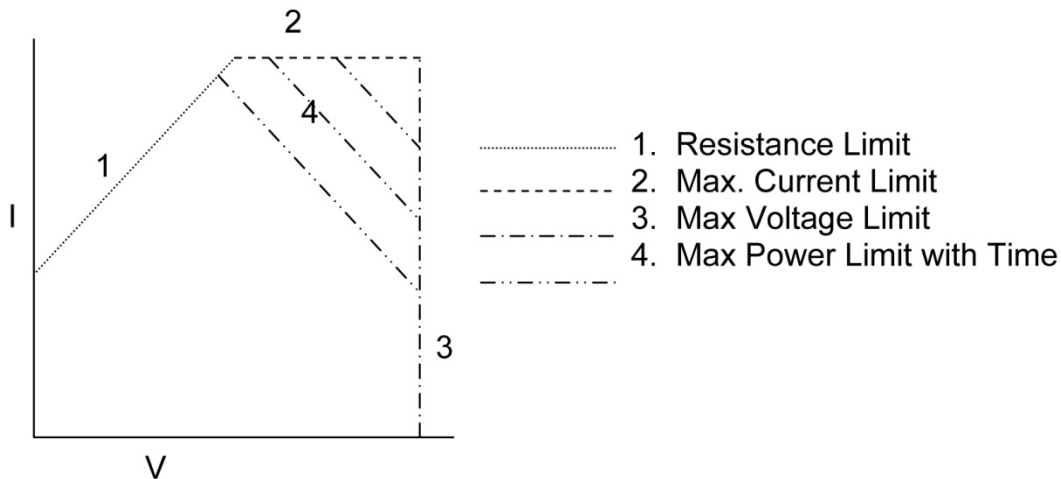At low gate voltages, conduction in MOSFETs is charge-carrier dominated. Charge-carrier concentration increases at higher temperatures and positive feedback allows thermal runaway. At high gate voltages, MOSFETs are mobility dominated. The charge-carriers mobility decreases as temperature increases.

Mobility carriers are less mobile at high temperatures. In older devices, the mobility effect "RULED" over the SOA. Today, charge carriers effect spill over from the right side of the SOA.

3.0 A Derivation of the Stability Criterion for Thermal Runaway, and the Spirito Effect

3.1 Purpose

The purpose of this section is to discuss the conditions under which thermal runaway can happen to a power MOSFET.

Subsection 3.2 considers only the case that the die is perfectly uniform over each vertical cross section.

In following sections, localized imperfections are shown to result in the formation of a 'hot spot' — a zone extending over only a few neighboring cells — that rapidly heats to destruction.

3.2 Uniform Cross Sections

If the device, and especially the die inside, is uniform from edge-to-edge over each vertical cross section in all its material properties and construction properties, There is particular interest in the temperature of the top surface of the die, T_j, where the Field-Effect Transistor (FET) channels occupy the upper few micrometers.[1]

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[1] Many semiconductor devices have a *pn*-junction, whose temperature affects the device's behavior; the 'junction temperature' T_j. An *n*-type FET has an *n*-conduction channel connecting an *n*-source to an *n*-sink; the cross-sectional area of this channel is changed by the electrical action of the gate. Hence, only material of the same type is active, and there is *no* 'junction' involved in this conduction.

3.2.1   Thermal resistance: part one

The temperature of the top surface of the die containing the 'sea' of FET-cells has an important effect on the behavior of the power MOSFET. Applied power deposits heat into this surface, while the thermal conductance of the die (and die attach, etc.) conducts heat from this surface: its temperature at the time t is a function of the history of the power applied up to the moment t. One particular history is to fix the case temperature T_c to a constant value (using sufficiently aggressive thermal clamping of the case) and wait until the entire device is at this case temperature. Then, apply a constant power P to the device, starting at $t = 0$ and continuing. The ratio of the rise in temperature of the top surface, T_j, to the applied power P is defined as the thermal resistance between 'junction' and case of the device:

$$R_{th}(t) = \frac{T_j(t) - T_e}{P} \tag{1}$$

This must begin at zero since $T_j(t = 0) = T_c$. It typically rises as $\sqrt{t}$ until the thermal pulse reaches the bottom of the case (this takes roughly h^2/D where h is the thickness of the die and D is the thermal diffusivity of silicon), after which it saturates to a constant value that is typically within a half-order of magnitude of 1°C/W.

Another particular history is to apply the power as a sequence of identical pulses with a fixed duty factor D. A duty factor of zero, $D = 0$, returns the 'single pulse' resulting in: $R_{th}(t|D = 0) = R_{th}(t)$. For a larger duty factor, the surface of the die is still somewhat heated by the previous pulses as the 'reference' cycle starts, as a result the value of $R_{th}(t|D > 0)$ starts at a higher value than zero; and $R_{th}(t|D = 1)$ is constant at its saturated value.

Most data sheets offer a plot of the thermal resistance for a sequence of 'constant power' pulses of various duty factors from $D = 0$ (the single pulse case) upward. See Figure 7 [1] for an example.
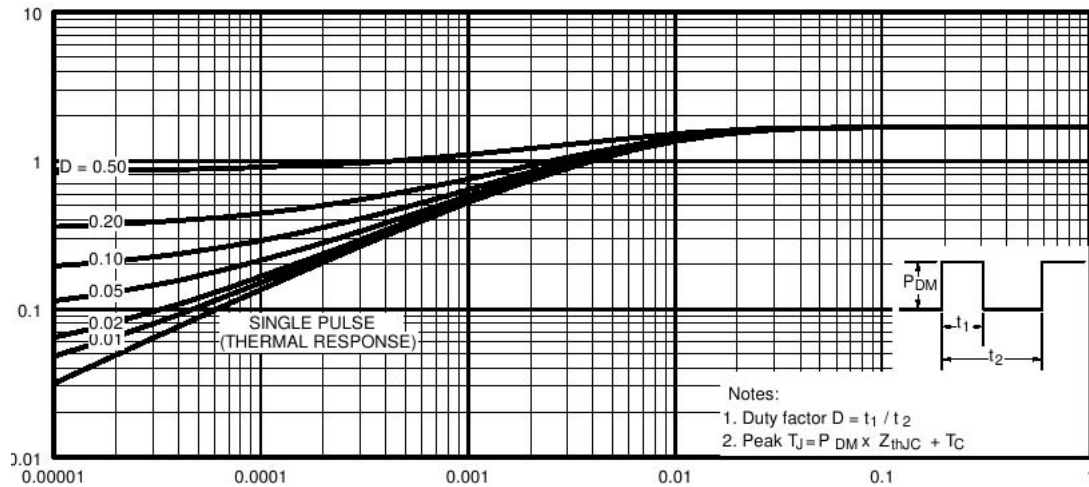
Figure 7. A typical plot of junction-to-case thermal resistance of a power MOSFET (IRF510). The horizontal axis is 'time t in seconds' when a constant power is dissipated; the vertical axis is 'temperature rise at the time t of the cells of the die per power deposited,' in °C/W; and the various curves are for various 'duty cycles.'

Other power-histories result in other behaviors of the temperature of the top surface $T_j(t)$: see section (below).

3.2.2　Curve traces

- plot of I_d vs V_d and V_g

- concentration on region for large V_d: saturation of I_d vs V_d, so I_d depends(almost) entirely on V_g

- re-plot of I_d vs V_g at various values of T

- observation that dI_d/dT can be positive

- re-plot of I_d vs T at fixed V_g, and observation of Taylor's series

3.2.3　Derivation of the condition of thermal runaway

The dependence of the drain current on gate voltage is modeled with usable accuracy by a linear function:

$$I_d(V_d, V_g, T_j) = I_d(V_d, V_g, T_c) + \alpha(V_d, V_g, T_c) \cdot (T_j - T_c) \tag{2}$$

$$\alpha(V_d, V_g, T_c) = \left[\frac{\partial I_d}{\partial T}\right]_{V_d, V_g} \tag{3}$$

The notation will be frequently simplified by suppressing the independent variables, using $I_d^{[c]} = I_d(V_d, V_g, T_c)$, $R_{th} = R_{th}(t)$ and $\alpha = \alpha(V_d, V_g, T_c)$

What happens as power is applied at constant drain and gate voltages can be anticipated, when $\alpha > 0$. As the junction temperature rises, the current rises increasing the power dissipated in the junction, which increases its temperature even more causing an additional rise in current. If this 'positive feedback' is large enough, the junction temperature can runaway to a disastrous value.

Holding the drain and gate voltages constant, the rise in the junction temperature is computed as follows:

$$T_j(t) - T_c = R_{th}(t) \cdot P(t) \tag{4}$$

$$= R_{th}(t) \cdot V_d \cdot I_d\left(V_d, V_g, T_j(t)\right) \tag{5}$$

$$= R_{th}(t) \cdot V_d \cdot \left[I_d^{[c]} + \alpha \cdot \left(T_j(t) - T_c\right)\right] \tag{6}$$

$$= R_{th}(t) \cdot V_d \cdot I_d^{[c]} + R_{th}(t) \cdot V_d \cdot \alpha \cdot \left[T_j(t) - T_c\right]. \tag{7}$$

or

$$\left[T_j(t) - T_c\right] \cdot [1 - R_{th}(t) \cdot V_d \cdot \alpha] = R_{th}(t) \cdot V_d \cdot I_d^{[c]}, \tag{8}$$

and this gives the 'large enough' result:

$$T_j(t) - T_c = \frac{R_{th} \cdot V_d \cdot I_d^{[c]}}{1 - R_{th} \cdot V_d \cdot \alpha} \tag{9}$$

The numerator is the temperature rise that would happen if the power were held constant[2] at $P^{[c]} = V_d \cdot I_d^{[c]}$. The denominator determines occurrence of thermal runaway. The term $R_{th}(t) \cdot V_d \cdot \alpha$ is zero at the start, $t = 0$, and increases with time. If it remains less than unity, the rise in the temperature of the junction, $T_j(t) - T_c$, remains bounded; however, the junction temperature $T_j(t)$ diverges to infinity if the term approaches unity. See Figure 8 [1].

To define the dimensionless stability factor S:

$$S = S(t, V_d, V_g, T_c) = R_{th}(t) \cdot V_d \cdot \alpha(V_d, V_g, T_c) = R_{th} \cdot V_d \cdot \alpha \tag{10}$$

Then Equation 9 states that the temperature of the surface of the die is bounded to a finite value when $S < 1$, and diverges to infinite values when $S \geq 1$:

$$S < 1: \; T_j \text{ is bounded,} \tag{11}$$

$$S \geq 1: \; T_j \text{ diverges to infinity.} \tag{12}$$

This is the condition celebrated by P. Spirito, and shown by him [4] (and by a number of others as well) to mark a curve on the SOA beyond which power MOSFETs show thermal runaway ending in catastrophic failure[3]. These are called Spirito-mode failures.
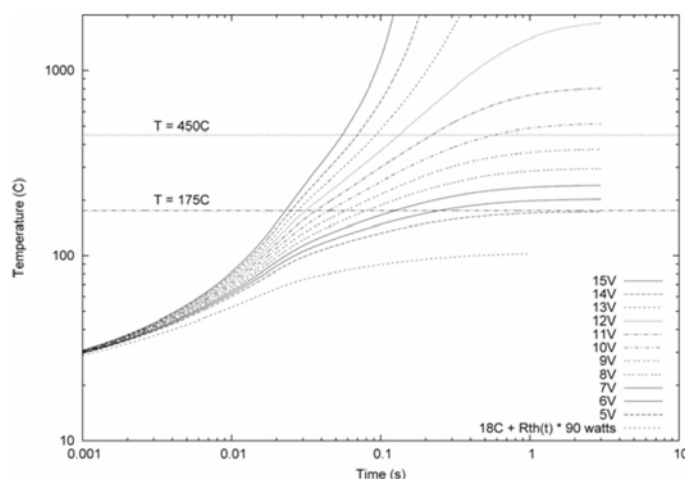
Figure 8. Illustration of the rise in T_j as the drain voltage V_d is increased in steps from 5 V to 15 V, and the gate voltage V_g at each step is held constant at a value that makes the initial value of drain current $I_d = 90$ W/V_d. Note that T_j diverges when V_d is between 12 V and 13 V. Also shown is the rise in T_j at a constant power of 90 W: $T_j(t) = 18°C + R_{th}(t) \cdot 90$ W. Values are for 'device 1' in Reference [4].

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[2] This is not strictly true, since the thermal resistance actually has a temperature dependence, decreasing as the junction temperature increases; precise modeling must take this into account.

[3] This criterion for thermal runaway is attributed by Marie Denison (et al.; [2]) to P. L. Hower and P. K. Govil [3].

The surface of the die need not reach an infinite temperature in order to be destroyed. Silicon melts at 1410ºC. The aluminum traces are melted at 660ºC and the eutectic temperature of aluminum-silicon alloys is 577ºC. The aluminum traces on the surface of the die interdiffuse with the silicon below 577ºC, and the time for this to become destructive is temperature dependant; there is enough interdiffusion at 450ºC that a few minutes at this temperature is used to obtain low contact resistance for Al-Si contacts. On the other hand, a few hours at 400ºC has no effect. FET manufacturers generally list 150ºC or 175ºC as the absolute maximum temperature T_j^{AbsMax} for the complete device; none mention the median time to degradation.

In summary, failure by 'cooking' the top surface can happen while S is less than unity: divergence of T_j is not actually required. Having $S < 1$ does not guarantee the device is being operated safely; rather, the stability factor must be sufficiently less than unity that T_j never approaches 450ºC, and users should require that T_j never exceeds the manufacturer's value for T_j^{AbsMax}.

Figure 8 shows that $T_j = 450$ºC is reached at slightly less than a second at $V_d = 9$ V for Spirito's device 1 (described in Reference [4]), and at about a tenth of a second at 12 V; however, divergence to infinite temperatures does not happen until V_d exceeds 12 V. The drain voltage must be 5 V (or less) to ensure T_j remains less than 175ºC. Hence, ignoring the small increase in thermal resistance after 0.1 second. Devastating interdiffusion could happen when $S \approx (9 \text{ V}/12 \text{ V}) = 0.7$, and caution in this case requires $S \lesssim (5 \text{ V}/12 \text{ V}) = 0.4$.

Clamping the voltages V_d and V_g, and the case temperature T_c, does not clamp the drain current I_d or the power $P = V_d \cdot I_d$ to constant values. The drain current and the power change with the changing temperature of the surface of the die, $T_j(t)$, result in:

$$T_j(t) = T_c + \left[R_{th}(t) \cdot P^{[c]} \cdot \frac{1}{1-S} \right], \tag{13}$$

$$I_d(t) = I_d^{[c]} + \frac{R_{th}(t) \cdot P^{[c]} \cdot \alpha}{1 - R_{th}(t) \cdot V_d \cdot \alpha} = I_d^{[c]} \cdot \left[\frac{1}{1-S} \right], \tag{14}$$

and

$$P(t) = V_d \cdot I_d(t) = P^{[c]} \cdot \left[1 + \frac{R_{th}(t) \cdot V_d \cdot \alpha}{1 - R_{th}(t) \cdot V_d \cdot \alpha} \right] = P^{[c]} \cdot \left[\frac{1}{1-S} \right] \tag{15}$$

The usual method of reporting a SOA by using the drain current as the vertical axis is misleading The device does not continue to operate at the same V_d-, I_d-point when thermal runaway happens; rather, this point becomes a vertical trajectory. It may start at a region that is 'safe' (in that T_j would always remain below T_j^{AbsMax} if I_d retained that original value) but then move into a region that 'cooks' the die. Thus, the set of starting V_d-, I_d-points that always stay 'safe' must be identified as they evolve with time, and plotted on the SOA diagram.

3.2.4   Hot Spots

The criterion for thermal runaway, $S \geq 1$, is derived above on the assumption that the entire surface of the die is heating uniformly. Indeed, a uniform die is the condition for defining the thermal resistance $R_{th}(t)$ that appears in the criterion.

Actual devices do not have cross sections that are rigorously uniform in properties and behaviors. There are often voids in the die attach. When a void is larger than roughly the thickness of the die, it substantially increases the thermal resistance of the path starting at the die's surface and passing vertically thru that void to get to the case. There are also local variations in doping and fabrication-geometry that result in some cells having a higher threshold voltage; such cells conduct less current than others with lower threshold voltage. The current-supply leads bonded to the top of the die provide an additional thermal path to case, and thus lower the thermal resistance of the zone at and around each lead attachment location. A large enough pulse of drain current flooding into the aluminum traces on the surface of the die can induce a local voltage drop across these traces so that V_d is larger in the zone where the current-supply leads are attached. Thus, S does not have a constant value over the cross section of an actual die. Even when S is safely less than unity across most of the die's cross-section, it may still be unsafe at some particular zone. This can be a source of part-to-part variations in resistance to Spirito-mode failures.

As the entire surface begins heating into a thermal runaway process per the Spirito-mode, some zones will heat faster than the typical zone; one of these will develop into a *hot spot*. It will 'hog' current from its neighbors (all at the same applied V_d and V_g) allowing it to accelerate beyond them toward dangerously high temperatures. Inspection of the destroyed device shows a small melted zone.

Much of the literature discussing Spirito-mode failures calls attention to the development of these hot spots and may give the impression that they are the cause of this class of failures instead of a natural consequence of the final moments of the process. However, obtaining devices that are completely free of non-uniformities would not eliminate the Spirito-mode failure, which is present (per Equation 9) even in a completely uniform device.

4.0   Effect of β on the Spirito Criterion for Thermal Runaway of a Power MOSFET

4.1   Apply Power: The MOSFET Heats

One way to apply power to a power MOSFET is to hold constant both the drain voltage V_d and the drain current I_d. (This requires changing the gate voltage V_g as the die heats.) The power deposited into the 'sea of FETs' on the surface of the die is then a constant, $P = V_d I_d$, and the temperature of the 'sea' is given by the thermal resistance $R_{th}(t)$:

$$T(t) = T(0) + R_{th}(t)P = T(0) + R_{th}(t)V_d I_d \tag{16}$$

This power can be applied until the 'sea' heats to a dangerous extent; heating longer will damage the device. There is a relationship between what maximum temperature is 'safe' (i.e., the device will be unchanged when it returns to a normal temperature) or 'unsafe,' and the duration of the time the 'sea' is held at that high temperature. If the duration is less than a microsecond, then perhaps reaching 350°C is safe. If the duration is longer than seconds, then perhaps 175°C is safe; but, some manufacturers report $T_{safe} = 150°C$. Using the latter value and $T(0) = 25°C$, the time (t_{safe}) during which the power can be applied, while limiting the temperature rise to the 'safe' value, is found by solving:

$$R_{th}\left(t_{safe}\right) = \frac{125°C}{I_d V_d} \tag{17}$$

An estimate of the thermal resistance $R_{th}(t)$ is derived from the data sheet for the part, and the inter-relationship between t_{safe}, I_d and V_d can be used to draw the 'safe power' line on the SOA diagram.

A different way to apply power to a MOSFET is to maintain both the drain voltage V_d and the gate voltage V_g constant. As the 'sea' heats, the drain current changes (determined by curve tracing at various temperatures). If the drain current decreases with increasing temperature, the device is stable. The contrary means the device can suffer 'thermal runaway.'

If the dependence of the drain current is described using a Taylor's series:

$$I_d(V_d, V_g, T) = I_d^{[0]} + \alpha \cdot (T - T_0) + \beta \cdot (T - T_0)^2 + O(3), \tag{18}$$

where

$T_0 = T(0)$ is the temperature, such as 25°C, of the 'sea' at $t = 0$.

$I_d^{[0]} = I_d(V_d, V_g, T_0)$.

$\alpha = \dfrac{dI_d}{dT}$ evaluated at V_d, V_g, T_0.

$\beta = \dfrac{1}{2}\dfrac{d^2 I_d}{dT^2}$ evaluated at V_d, V_g, T_0.

If $\beta \cdot (T - T_0)^2$ is small enough compared with $\alpha \cdot (T - T_0)$, the 'β'-term can be ignored.

Then algebra gives:

$$T(t) - T_0 = \frac{R_{th}(t) V_d I_d^{[0]}}{1 - S}, \tag{19}$$

where $S = \alpha V_d R_{th}(t)$ is the Spirito stability factor, and where the affect of the time-changing power on the thermal resistance is thought to be ignorable. As $S \to \infty$, the temperature diverges to infinite values; this is an unstable case. For this to happen, α must be positive (the drain current I_d must increase with increasing temperature)and α must be sufficiently positive that the triple-product S approaches unity.

The power MOSFET is unsafe long before $S \to \infty$. All that is necessary is $T(t)$ reach T_{safe}. This happens when

$$R_{th}(t_{safe}) = (1 - S) \cdot \left[\frac{T_{safe} - T_0}{V_d I_d^{[0]}} \right]. \tag{20}$$

The 'safe' time is reduced when $\alpha > 0$ and increased when it is negative.

If $\beta \neq 0$, then

$$T(t) - T_0 = \left[\frac{R_{th}(t) V_d I_d^{[0]}}{1 - S} \right] + \frac{\beta}{I_d^{[0]}} \cdot \left[\frac{R_{th}(t) V_d I_d^{[0]}}{1 - S} \right]^3 \tag{21}$$

This expression reduces to the when $\beta \to \infty$ and it has the singularity at precisely the same condition ($S \to \infty$). The numerical details are affected by whether β is positive or negative.

This expression can be solved for the time t_{safe} this 'sea' takes to reach T_{safe}.

Note: the modeling of $T(t)$ and of t_{safe} have been improved by including β, but the modeling has been degraded in a different way: once the drain current I_d depends on time, the power dissipated into the 'sea' is not constant with time; rather, this power may increase ($\alpha > 0$) or it may decrease ($\alpha < 0$) during the pulse. This means the temperature is no longer given by Equation 17. Recomputing must be done to find the 'correct' heating of the 'sea.'

5.0   MOSFET Testing Results and Information Dissemination

5.1   Nondestructive Test for MOSFET Thermal Instability

5.1.1   Assumptions Made

With an understanding of the failure mechanism, it is time to investigate what is needed to record actual test data. Theoretically, several assumptions are made about the beginning of the failure that are not proven at the end of the parts failure. Throughout the theoretical section, one underlying assumption (that is the assumption that the MOSFET heats evenly throughout the event) seems incorrect. Reviewing test data taken when the lid is removed, the MOSFET does remain uniform across the die to within ten percent. It is only when the part is starting to fail that the temperature deviates across the MOSFET. The second assumption being made is that the intrinsic diodes internal to the part show the temperature of the hottest point in the MOSFET when a small reverse current is applied to the intrinsic diodes. Again, this works well as long as the temperature remains uniform. Once a hot spot starts to appear, the temperature reported by the diodes start to fall off from externally made measurements. Unfortunately, methods used to read the temperature independent from the part require the part to be destroyed (delidded). With the exception of finding the thermal resistance, all testing is to be done while trying to avoid changing the temperature of the MOSFET above the starting point of the MOSFET. Lastly, it is assumed that all parts tested are to be tested non-destructively.

5.1.2   Data Needed From Test

The intent of the testing is to collect four sets of data. This data can be used to analyze the location within the SOA where a MOSFET will have thermal instability problems. The four sets are:

1. Temperature of the MOSFET (T).

2. The voltages on the MOSFET (V_d).

3. Current going through a MOSFET at known Gate voltages at different known temperatures (I_d).

4. Thermal Resistance; the temperature increase for a given power for a given period of time (R_{th}).

Test Equipment

While it would be very easy to state the steps used to determine these values, a more generic description is being attempted to avoid the need for having any specific piece of equipment.

Note to determine α and even β, voltage and current are needed at the same time. An IV curve tracer servers the purpose well if it is modified to drive the test parts to different temperatures.

MOSFET Temperature

All measurements need to originate from the MOSFET's internal temperature. With one exception, the temperature required is located inside the sealed part, hidden from direct observation. This exception is the die itself. The intrinsic diode (part of all MOSFETs) can be used to determine the temperature of the MOSFET. A schematic for intrinsic diode temperature measurement is shown in Figure 9. By placing a small negative current (1mA to 10mA.) between the Drain and Source, a voltage can be read that correlates with the temperature. The voltage change should be near 0.002 volts per °C for a 10mA source. The actual voltage change can be determined by running the test-current source through the intrinsic diodes at several known temperatures, and building up a table of the temperatures and voltages, or by determining the slope and offset of the function. The temperature should be well controlled, and there should be no power in the MOSFET other than the 10mA test current. If air is being used to control the temperature of the part, the part should be monitored to determine when the part is in equilibrium with the moving air. Equalizing the part's temperature and the air stream may take up to 20 minutes per temperature step and should be verified by the internal current (voltage) measurement. At a minimum, verified temperature measurement should be made at 0°C, 25°C, and 100°C. Other temperature measurements can be extracted from the voltage measurements.
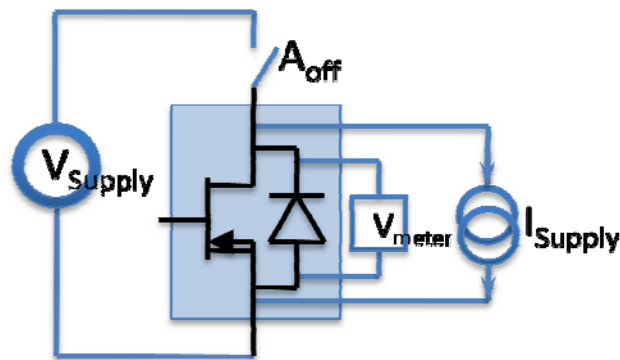

Figure 9. Simplified schematic for intrinsic diode temperature measurement.

Voltage in the Device at Set Temperatures

With a way of knowing the internal MOSFET temperature, being able to determine the Drain to Source voltage is required. The same meter can be used for both temperature and voltage if a second switch is employed to stop the main current following the test time. This is needed due to the reversal in current. The temperatures will read as negative voltages and the V_{ds} voltage will appear positive. The meter used is required to take measurements very quickly and hold the reading. The intention of the short measurement times is to reduce the amount of heat built up in the MOSFET. For voltage and current measurements at temperature, heating of the MOSFET needs to be kept to a minimum. Increases in temperature should be less than twice the noise floor of the voltmeter (5°C over a series of test pulses, 10 pulses in 10 seconds). To keep the temperature unchanged, the test pulses should be limited to approximately 20uSec. Voltage probe points should be as close to the test MOSFET as possible, and the probes should not be used to carry current. These need to be Kelvin connections.

Along with using Kelvin connections, it is necessary to have a very stiff voltage supply. With resistances being very low for the total circuit and low on resistances internal to the part, large capacitors close to the switches is recommended. A large capacitor will help lower the need for heavy wire running to a power supply

Depending on the method of taking the voltage there may be a problem with the measurements. Most oscilloscopes are limited in voltage measurements to values that are on the screen. If the trace goes off screen the values become saturated, requiring time for the scope to recover once the signal is back on the screen. The oscilloscope's recovery time can be verified by the manufacturer. Signals that fall within this time interval will be in error, and cannot be used or trusted. Using a single channel set to a large voltage level to capture both the temperature reading and the V_{ds} value will increase the noise in the temperature readings. The use of two channels may provide a better solution. If a smaller scale is used for the temperature reading a small signal diode and large resistor can be used to block the higher forward voltage.

Current at the Set Temperature

The current required is the current flowing through the MOSFET (I_d). A schematic for I_d current measurement can be seen in Figure 10. The use of a large capacitor in the system not only helps with holding the voltage stable, but also allows the current to flow by reducing the total impedance path during the on pulse. The current reading needs to be taken inside of the capacitor, MOSFET circuit. A current shunt could be used if it is of sufficient size to allow for high currents (20 A to 30 A). However, a current shunt will add resistance to the over all system, and could easily double the resistance of the circuit. For this reason a current probe is recommended.
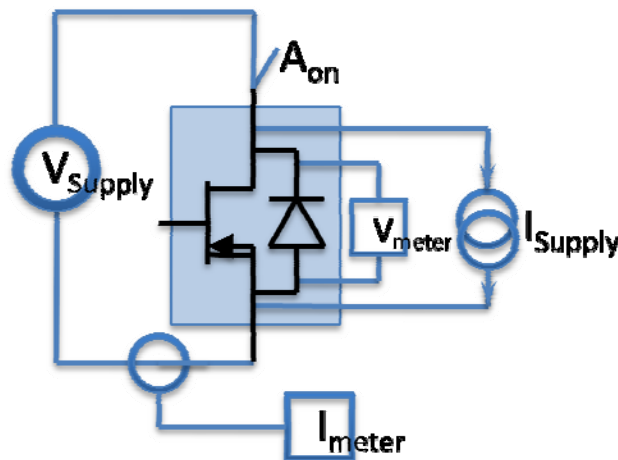

Figure 10. Simplified schematic for I_d current measurement.

Thermal Resistance

Thermal resistance is a time dependant measurement of the temperature of the MOSFET die with a given power input. For short periods of time the change in temperature remains in the die itself. With slightly longer periods of time the temperature rise will travel out of the die into the base of the part. This process is repeated again for the heat traveling into the printed circuit (PC) board, and then again into the PC board's heat sink. The manufacturer has no way of knowing the thermal path outside of their part's case and cannot advertise the total thermal resistance for time periods greater than 1 second. It is the total thermal resistance that is required if the part is being used for long time periods. It should also be noted that some MOSFET thermal resistance charts have been found to be incorrect for the stated parts.

5.2   Test Data Development of Data

With the four sets of data discussed in Section 3.1.2, it is possible to record values for α and β. With this data, the Spirito Stability Criteria can be determined.

It should be noted that α and β are curves as a function of V_{gs} or even I_d. For derating of the stability criteria, the maximum values of α and β should be used. Testing to date has shown β to be about 100 times smaller in value from α.

5.2.1   Alpha

If a curve tracer has been used, α can be found by selecting a voltage common to two temperature data sets and gate voltages, subtracting the lower temperature data point from the higher temperature data point, and dividing by the temperature difference of the two data points. The α curve will be the collection of current differences verses the gate voltages. The temperature steps used should be limited to no greater than 25ºC. Smaller temperature steps would be better.

5.2.2   Beta

If α is found over a series of temperature steps, β will be the differences in α with an increase in temperature.

6.0   Executive Summary

Based on recent testing and failure investigations, it appears the "old" SOA application curves are inaccurate with regard to the SOA of some MOSFET parts. These parts are used extensively in flight hardware and ground support equipment.

With the push for faster switching, lower on resistance power MOSFETs, came an unintended consequence similar to, but not seen since the prime of the bipolar transistor, which was the secondary voltage breakdown effect. While MOSFETs are in the charge-carrier dominated region (low V_{gs}) the MOSFET allows more current to flow as the temperature increases causing a thermal runaway. It was discovered that the SOA curves given by the manufacturers were lacking in giving the region of thermal instability. A review of papers from the automotive industry is described, and recommendations to add the area of thermal instability are included. The four factors that are important in determining the thermal instability are:

1. α defined as the change in current over the change in temperature. (dI/dT)

2. β defined as the acceleration of current over the change in temperature. ($d**2*I/dT**2$)

3. Thermal resistance of the surface of the MOSFET which is the change in temperature over the power in the part.

4. The voltage across the MOSFET from the Drain to the Source.

7.0   References

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The NESC provided support after the recent discovery of Power MOSFET failures and the need to update the safe operating range as opposed to relying solely on the manufacturer's application curves. This report was prepared in support of NESC Request# TI-09-00505; Power MOSFET Thermal Instability Operation Characterization Support.

14. ABSTRACT

Metal-oxide semiconductor field-effect transistors (MOSFETs) are used extensively in flight hardware and ground support equipment. In the quest for faster switching times and lower "on resistance," the MOSFETs designed from 1998 to the present have achieved most of their intended goals. In the quest for lower on resistance and higher switching speeds, the designs now being produced allow the charge-carrier dominated region (once small and outside of the area of concern) to become important and inside the safe operating area (SOA). The charge-carrier dominated region allows more current to flow as the temperature increases. The higher temperatures produce more current resulting in the beginning of thermal runaway. Thermal runaway is a problem affecting a wide range of modern MOSFETs from more than one manufacturer. This report contains information on MOSFET failures, their causes and test results and information dissemination.

15. SUBJECT TERMS

Metal-oxide Semiconductor Field-effect Transistors; Thermal Runaway; Safe Operating Area; Field-Effect Transistor

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